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09.857,569	06-07/2001	Masatake Nakano	109715	5019

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EXAMINER

GOUDREAU, GEORGE A

ART UNIT PAPER NUMBER

1763

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09-857569

Applicant(s)

Nakamura et al.

Examiner

George Goudreau

Group Art Unit

1763

— The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on (6-01-03 to 3-02-03) (ie. - papers # (1-5))

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 10-24 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 10-16, 20-24 is/are rejected.

☒ Claim(s) 17-19 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____

☐ Copies of the certified copies of the priority documents have been received
in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 5

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

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15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 C of this title before the invention thereof by the applicant for patent.

16. Claims 1-16, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Henley et. al. (6,265,328).

Henley et. al. disclose a process for forming an SOI structure on a wafer which is comprised of the following steps:

- An SOI structure is formed on a wafer using a Smart-Cut method. The SOI structure is comprised of a laminate of a Si film (14)/ a SiO₂ film (14, 18)/ bulk Si wafer (12).; and
- An exclusion zone of 5 mm is formed in the Si film (14) used to form the SOI structure using any of a variety of different methods. A etch mask (201) may be used in the wet etching or dry etching of the Si film (203) to form an exclusion zone. Alternatively, the Si film (411) may be ablated to form an exclusion zone using an ablation tool while supplying a wet or dry etchant to the surface of the Si film (411).

This is discussed specifically in columns 3-8; and discussed in general in columns 1-12.

This is shown in figures 1-6.

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17. Claims 10-16, 20, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Akino et. al. (6,417,108).

Akino et. al. disclose a process for forming a stepped shaped SOI structure on a wafer which is comprised of the following steps:

- An SOI structure is formed on the wafer using a Smart Cut method. The SOI structure is comprised of a laminate of a Si film (3)/ a SiO₂ film (2)/ bulk Si wafer (1).; and
- A stepped shape SOI structure is formed by using an etch mask (4, 6) to pattern the Si film (3), and the SOI film (2) in either a dry or wet etching step. Typically the Si film is removed (1.8 to 2.0) mm from the edge of the bulk Si wafer using such a method.

Alternatively, a cmp polishing process may be used to form the step shaped structure.

This is discussed specifically in columns 4-13; and discussed in general in columns 1-18.

This is shown in figures 1-13.

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made

19. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

20. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akino et. al. as applied in paragraph 17 above.

Akino et. al. as applied in paragraph 17 above fail to disclose the following aspects of applicant's claimed invention:

-the usage of a cmp polishing process to remove the Si film to the specific extent which is claimed by the applicant from the periphery of the wafer

It would have been obvious to one skilled in the art to remove the Si film to the specific extent from the wafer edge which is claimed by the applicant in the etching process which is taught above based upon the following. It would have been desirable to remove enough of the Si film from the periphery of the wafer to form an adequate step in the SOI structure formed on the wafer in the process taught above.

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21. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et. al. as applied in paragraph 16 above.

Henley et. al. as applied in paragraph 16 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a cmp polishing process to remove the Si film to the specific extent from the periphery of the wafer in the process taught above

It would have been obvious to one skilled in the art to employ a cmp polisher as the ablation tool in the process taught above based upon the following. The ablation of a substrate using a cmp polisher is conventional or at least well known in the cmp polishing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for conducting the ablation step in the process taught above to the specific usage of other such means.

It would have been obvious to one skilled in the art to remove the Si film to the specific extent from the wafer edge which is claimed by the applicant in the etching process which is taught above based upon the following. It would have been desirable to remove enough of the Si film from the periphery of the wafer to form an adequate exclusion zone in the SOI structure formed on the wafer in the process taught above.


22. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.


George A. Goudreau/gag

Primary Examiner

AU 1763